**Lab 4. Memory**

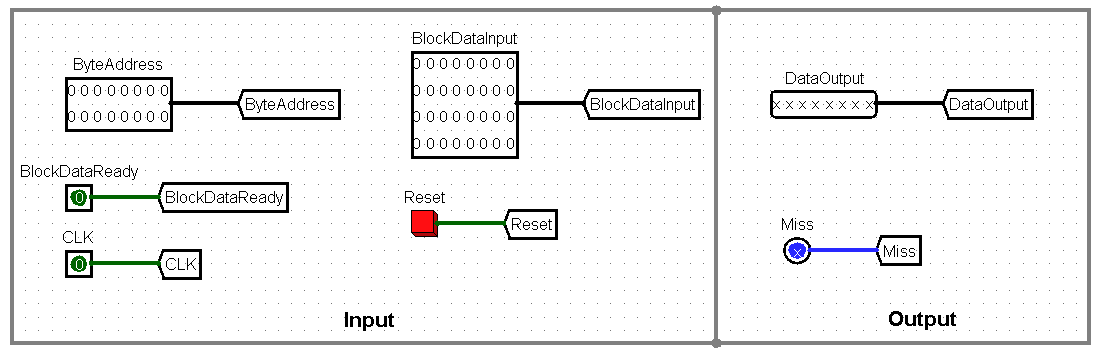
1. **Objectives:**
2. Learn how to design direct-mapped cache.
3. **Resources:**
4. Download Logisim 2.7.1 from canvas
5. Download “Lab4 - Memory.circ” from Canvas. Inputs, outputs, and most of the necessary electronic components have been given in each circuit. **Do not make any changes to the given Inputs and outputs in the circuits, and Do not change the appearances of electronic components.**
6. **Requirements**

Write your answers to the questions in the following “4. Tasks” section in your lab report. Do not forget to show your demo to TA if required.

1. **Tasks**:

Design a direct-mapped cache. It has 8 blocks and the size of each block is 1 word. Data in the memory is byte addressed and the address width is 16 bits.

When the processor requests data with a “ByteAddress”, the cache should be able to determine whether this request is a hit or miss. If it is a hit, the requested byte should be sent to “DataOutput”. If it is a miss, the cache should store “BlockDataInput” to the corresponding cache block when “BlockDataReady” is asserted, then send the requested data to “DataOutput”.



**4.1 Design a direct-mapped cache (50 points)**

Explain your design method:

The BlockDataInput(32-bit), Tag(11-bit), and a constant 1(1-bit) go to a register which is enabled by it’s writeX. The output of the Tag and constant 1 registers get combined and get sent through a multiplexer selected by the index. Its output gets compared to a combined Tag and constant 1 that when equal, means a hit is achieved (and a miss when not). The Hit gets sent through a demultiplexer which is the switch of a controlled buffer meeting the output of the 32-bit, BlockDataInput registers. The outputs from all the controlled buffers get combined and enter a multiplexer. This multiplexer is selected by the bit offset and the Hit. The result from the multiplexer is the DataOutput.

Circuit:

Diagram, schematic

Description automatically generated

**4.2 Demo your design to TA (50 points)**

Note: Random testing cases will be used for testing your design during the demo.